January, 17, 2024

1 st Year Licence on computer science

Module: STRM1

Correction of the exam.

Exercise 1 (7 pts).

1) $A = (1A)_{16} = (00011010)_2 = (?)_{10}$.

$= 1.2^4 + 1.2^3 + 1.2^1 = 16 + 8 + 2 = (26)_{10}$. | 0,5

$B = (BC)_{16} = (10111100)_{C_2} = (?)_{10}$.

$(10111100)_{C_2} = (?)_2$

$|10111100| = 0111100$; $(0111100)'' = 1000011 + 1$

$= 1000100$.

$(10111100)_{C_2} = (11000100)_2 = 1.2^6 + 1.2^2 = (-68)_{10}$. | 0,75

$C = (55)_{16} = (01010101)_G = (?)_{10}$.

$(01010101)_G = (?)_2$

0 1 0 1 0 1 0 1
$G_8\ G_7\ G_6\ G_5\ G_4\ G_3\ G_2\ G_1$.

$B_8 = G_8 = 0$
$B_7 = G_7 \oplus B_8 = 1$
$B_6 = G_6 \oplus B_7 = 1$
$B_5 = G_5 \oplus B_6 = 0$
$B_4 = G_4 \oplus B_5 = 0$.
$B_3 = G_3 \oplus B_4 = 1$
$B_2 = G_2 \oplus B_3 = 1$.
$B_1 = G_1 \oplus B_2 = 0$.

0,5 $C = (01100110)_2 = (?)_{10}$

$= 1.2^6 + 1.2^5 + 1.2^2 + 1.2^1 = (102)_{10}$.

$D = (D9)_{16} = (11011001)_2 = (?)_{10}$ | 0,5

bit sign

$= 1.2^6 + 1.2^4 + 1.2^3 + 1.2^0 = (-89)_{10}$

$E = (C19A0000)_{16}$

$= \boxed{1}\boxed{10000011}\boxed{00110100000\ 0000\ 0000\ 0000}$

bit sign exp Mantissa

0,75

$exp_B = (10000011)_2 = (131)_{10} \Rightarrow exp = exp_B - 127 = 131 - 127$
$= 4.$

$E = -1,0011\,01 \times 2^4 = 10011,01 = 1.2^4 + 1.2^1 + 1.2^0 + 1.2^{-2}$
$= (-19,25)_{10}.$

2) $(-B)_{c_2} + (C)_{c_2} = ?$

$B = (10111100)_{c_2} \Rightarrow -B = ?$

$|-B| = 0111100\,;\ (0111100)'' = 1000011 + 1 = 1000100.$ 0,5

$-B = (01000100)_2 = (01000100)_{C_2}.$

$C = (01100110)_2 = (01100110)_{C_2}.$ 0,25

$(-B)_{c_2} + (C)_{c_2} = ?$

$$\begin{array}{r|l} & 0\ 1000100 \\ + & 0\ 1100110 \\ \hline & 1\ 0101010 \end{array}$$

1

bit sign

carry = 0

overflow? $(+) + (+) = (-) \Rightarrow$ there is an overflow. 0,25

3) $E + A = -1,001101 \times 2^4 + 00011010$

0,75

$= (-1,001101 + 1,1010) \times 2^4$

$$\begin{array}{r} 1,1010000. \\ -\ 1,0011101. \\ \hline 0,0111011 \end{array}$$

0,5

$E + A = 0,011011 \times 2^4.$
$= 1,1011 \times 2^2.$
$exp = 2 \Rightarrow exp_B = 127 + 2 = 129$
$= (10000001)_2$

$M = 10110$

in the machine 23 bits

$$\boxed{0 \,|\, 10000001 \,|\, 10110 - - - - - - . \,0.}$$

(0,75)

Condensed in base 16 ?

$$\underbrace{0100}_{4}\;\underbrace{0000}_{0}\;\underbrace{1101}_{D}\;\underbrace{1000}_{8}\;\underbrace{0000}_{0}\;\underbrace{0000}_{0}\;\underbrace{0000}_{0}\;\underbrace{0000}_{0}$$

$$E+A = (40D80000)_{16}$$

Exercise 2 :

A) 1) Expression of F :

$$F = \overline{\overline{(\bar{C} + A)} \cdot D + A \oplus B}$$

(1,5)

2) Simplified function of F.

$$F = (\bar{C} + A) \cdot D \cdot (\overline{A \oplus B}) = (\bar{C} + A) \cdot D \cdot (\bar{A}\bar{B} + AB).$$

$$= \bar{A}\bar{B}\bar{C}D + ABD(1 + \bar{C})$$

(1,5)

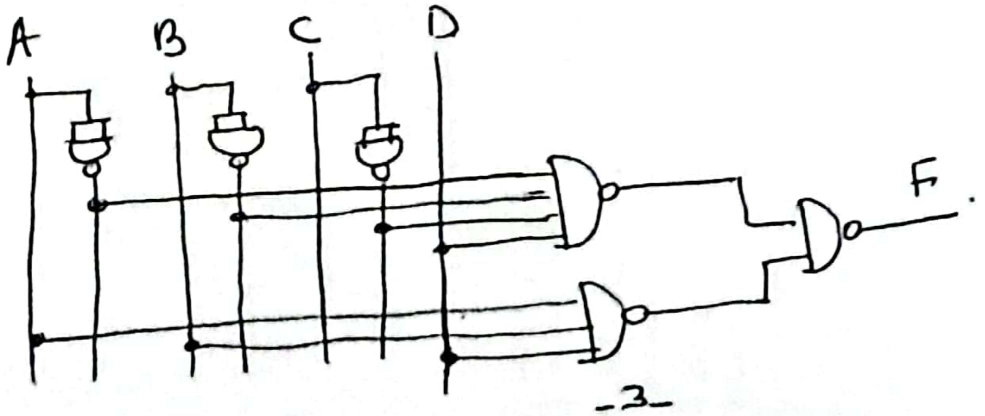
$$F = \bar{A}\bar{B}\bar{C}D + AB\bar{C}D + ABD.$$

$$\boxed{F = \bar{A}\bar{B}\bar{C}D + ABD}$$

3) Realization of the circuit with only NAND gates.

$$F = \overline{\overline{\bar{A}\bar{B}\bar{C}D + ABD}} = \overline{\overline{\bar{A}\bar{B}\bar{C}D} \cdot \overline{ABD}}$$

(1)



B)

1) $(X\bar Z + YZ) \oplus (X\bar Y + YZ) \overset{?}{=} X(Y \oplus Z)$

$= \overline{(X\bar Z + YZ)} \cdot (X\bar Y + YZ) + (X\bar Z + YZ)\overline{(X\bar Y + YZ)}$

$= \overline{X\bar Z} \cdot \overline{YZ} \cdot (X\bar Y + YZ) + (X\bar Z + YZ)(\overline{X\bar Y} \cdot \overline{YZ})$

$= (\bar X + Z) \cdot (\bar Y + \bar Z)(X\bar Y + YZ) + (X\bar Z + YZ)(\bar X + Y)(\bar Y + \bar Z)$

$= (\bar X\bar Y + \bar X\bar Z + Z\bar Y + \underbrace{Z\bar Z}_{0})(X\bar Y + YZ) + (X\bar Z + YZ)(\bar X\bar Y + \bar X\bar Z + Y\bar Z)$

$= ZX\bar Y + XY\bar Z = X(Z\bar Y + Y\bar Z) = \boxed{X(Z \oplus Y)}$

1

2) $F = \underset{1100}{AB\bar C\bar D} + \underset{1011}{A\bar B CD} + \underset{1111}{ABCD} + \underset{1110}{ABC\bar D} + \underset{0101}{\bar A B\bar C D} + \underset{0111}{\bar A BCD}$

simplification by Karnaugh-map.

AB \ CD	00	01	11	10
00				
01		1	1	
11	1		1	1
10			1	

$\boxed{F = AB\bar D + \bar A BD + ACD}$

1

Exercise 3 :

1) Truth Table

X_1	X_0	Y_1	Y_0	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

1

2) Simplification :

Z_0

$X_1X_0 \backslash Y_1Y_0$	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	0	1	1	0
10	0	0	0	0

$$\boxed{Z_0 = X_0 Y_0}$$ (0,5)

Z_1

$X_1X_0 \backslash Y_1Y_0$	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	1	0	1
10	0	1	1	0

(0,5)

$$\boxed{Z_1 = X_1 \bar{Y}_1 Y_0 + X_1 \bar{X}_0 Y_0 + \bar{X}_1 X_0 Y_1 + X_0 Y_1 \bar{Y}_0}$$

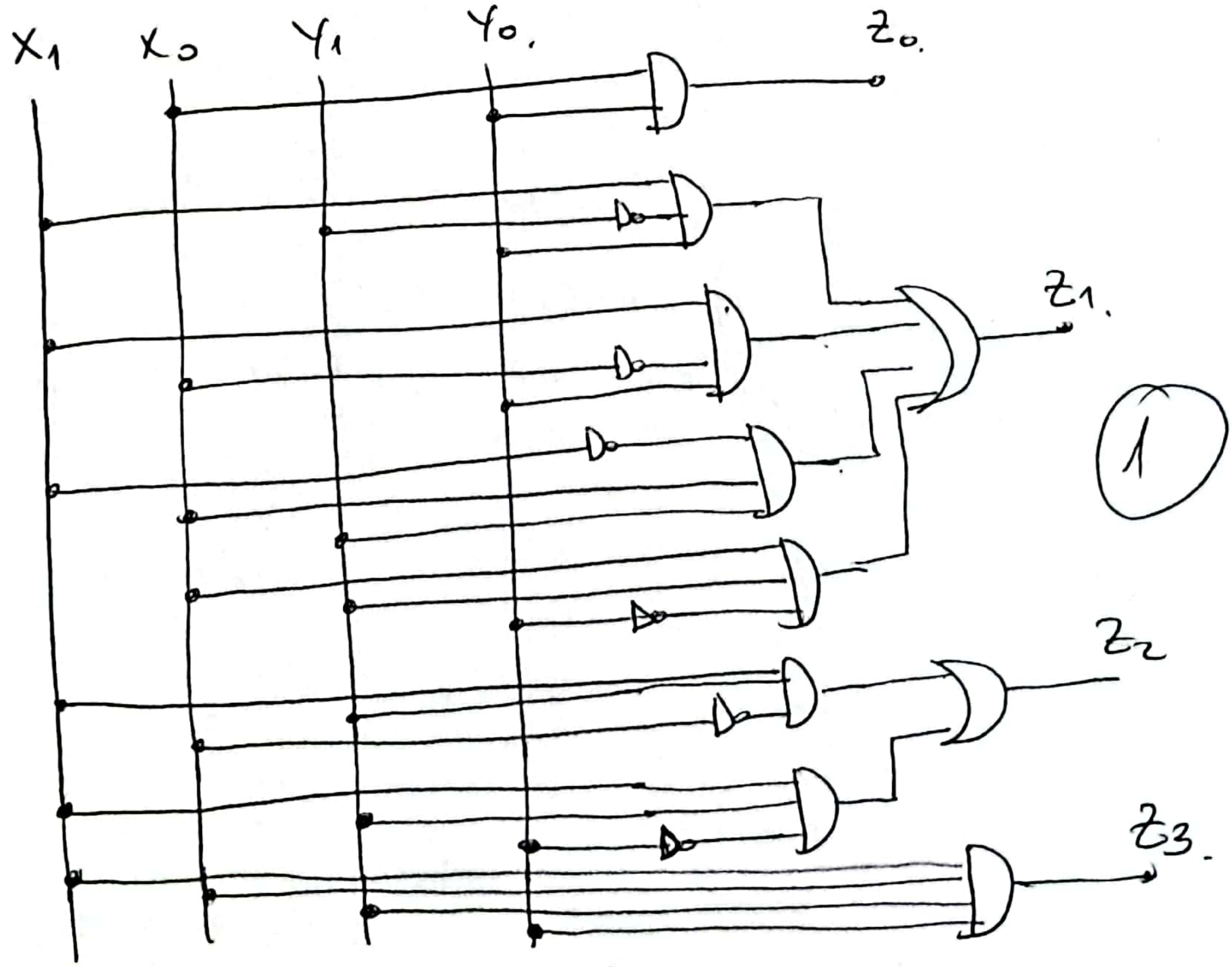
Z_2

$X_1X_0 \backslash Y_1Y_0$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	1
10	0	0	1	1

$$\boxed{Z_3 = X_1 X_0 Y_1 Y_0}$$ (0,5)

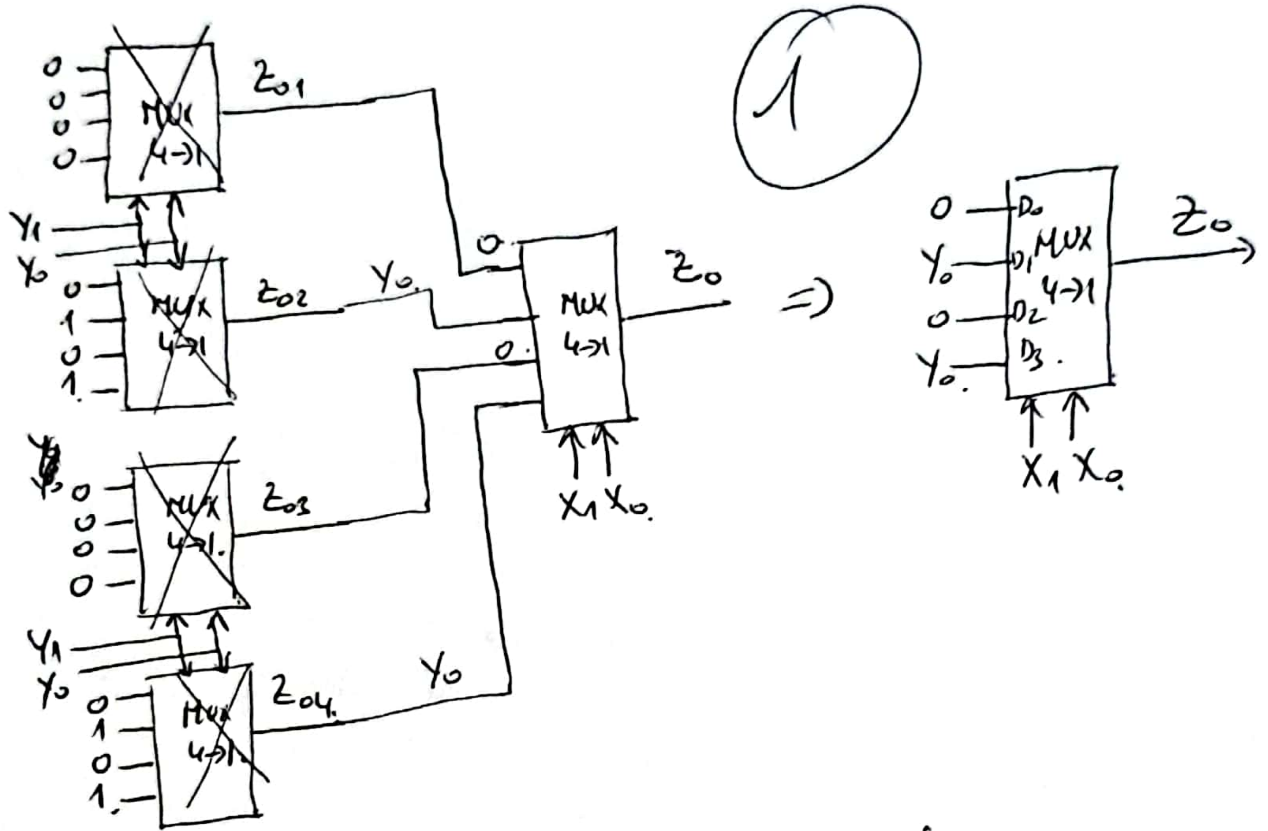
$$\boxed{Z_2 = X_1 \bar{X}_0 Y_1 + X_1 Y_1 \bar{Y}_0}$$ (0,5)

3) Diagram of the complete circuit :



4) Z_0 with a minimum of MUX 4→1 :

From the truth table we can deduce the following circuit of Z_0



5) Z_1 with a DEC 8→1 and Logic gates.

using simplified equation Z_1 :

$$Z_1 = X_1\bar{Y}_1Y_0 + X_1\bar{X}_0Y_0 + \bar{X}_1X_0Y_1 + X_0Y_1\bar{Y}_0$$

$$= X_1(\bar{Y}_1Y_0 + \bar{X}_0Y_0) + \bar{X}_1X_0Y_1 + X_0Y_1\bar{Y}_0$$

$$= X_1.(\underbrace{X_0\bar{Y}_1Y_0}_{S5} + \underbrace{\bar{X}_0\bar{Y}_1Y_0}_{S1} + \underbrace{\bar{X}_0Y_1Y_0}_{S3}) + \bar{X}_1\underbrace{X_0Y_1Y_0}_{S7} + \underbrace{X_0Y_1\bar{Y}_0}_{S6}$$

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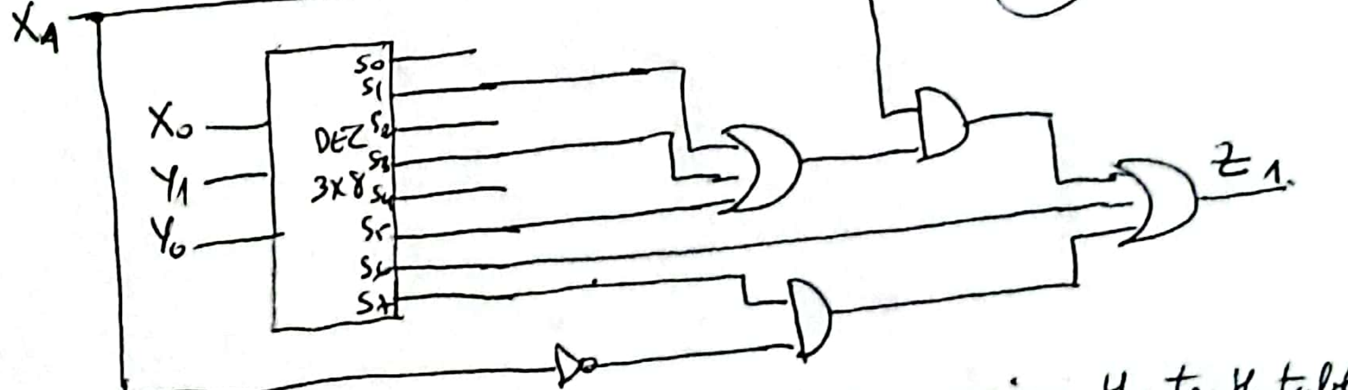
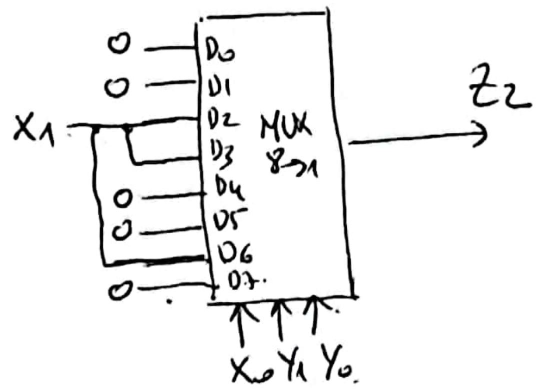


Remark : We can obtain the circuit by using the truth table also.

6) Z_2 with a MUX $8 \to 1$ and possible logic gates:

From the truth table we can deduce the following circuit of Z_2.



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